IN THE CLAIMS

The following list of claims replaces all prior versions, and listings, of claims in the application.

1. (Currently Amended) A method of recovering data from a modulated data signal, comprising:

tracking a transmitted clock with a plurality of locally-generated clock phases;

estimating an average phase of one or more ~~previously~~ detected edges in a data stream;

registering a pulse edge in the ~~received stream of~~ data stream, at a transition phase corresponding to one of said plurality of locally-generated clock phases;

determining whether a first symbol was received multiple times consecutively prior to the detected pulse edge; and

using the determination of whether said first symbol was received multiple times consecutively in a receiver decision process.

2. (Original) The method according to claim 1, wherein said determining includes determining whether the pulse edge registered during said registering step corresponds to a lone transition from a consecutive sequence of said first symbol to a second symbol.

3. (Original) The method according to claim 2, further comprising establishing a threshold number of consecutive symbols to precede any said lone transition.

4. (Currently Amended) The method according to claim 3, wherein, if the registered pulse edge is determined to correspond to said~~a~~ lone transition, said using comprises associating said registered pulse edge with a current bit period when a number of consecutively received symbols is below said threshold number of consecutive symbols and said transition phase precedes an eye opening formed in the data stream~~received data signal~~.

5. (Currently Amended) The method according to claim 3, wherein, if the registered pulse edge is determined to correspond to saida lone transition, said using comprises associating said registered pulse edge with a subsequent bit period when a number of consecutively received symbols is below said threshold number of consecutive symbols and an eye opening formed in the ~~received~~ data streamsignal precedes said transition phase.

6. (Currently Amended) The method according to claim 3, wherein if the registered pulse edge is determined to correspond to saida lone transition, said using comprises associating said registered pulse edge with a current bit period when a number of consecutively received symbols exceeds said threshold number of consecutive symbols and an eye opening formed in the ~~received~~ data streamsignal is between said transition phase and an immediately subsequent clock phase.

7. (Currently Amended) The method according to claim 1, wherein said determining includes determining whether the pulse edge registered during said registering step corresponds to a trailing edge of a single second symbol between a consecutive sequence of said first symbol and another occurrence of said first symbol.

8. (Currently Amended) The method according to claim 7, further comprising establishing a threshold number of consecutive symbols to precede saida single second symbol.

9. (Currently Amended) The method according to claim 8, wherein, if the registered pulse edge is determined to correspond to saida trailing edge of saida single second symbol, said using comprises associating said registered pulse edge with a current bit period when a number of consecutively received symbols is below said threshold number of consecutive symbols and said transition phase precedes an eye opening formed in the ~~received~~ data streamsignal.

10. (Currently Amended) The method according to claim 8, wherein, if the registered pulse edge is determined to correspond to saida trailing edge of saida single second symbol, said

using comprises associating said registered pulse edge with a subsequent bit period when a number of consecutively received symbols is below said threshold number of consecutive symbols and an eye opening formed in the ~~received~~ data streamsignal ~~signal~~ precedes the transition phase.

11. (Currently Amended) The method according to claim 8, wherein if the registered pulse edge is determined to correspond to saida ~~a~~ trailing edge of saida ~~a~~ single second symbol, said using comprises associating said registered pulse edge with a subsequent bit period when a number of consecutively received symbols exceeds said threshold number of consecutive symbols and an eye opening formed in the ~~received~~ data streamsignal ~~signal~~ is between said transition phase and an immediately subsequent clock phase.

12. (Currently Amended) An edge processor adapted to determine an average phase of detected edges and output a data signal and saidan ~~an~~ average phase, said edge processor comprising:

a synchronizer operative to compare a detected edge signal to a plurality of locally generated clock phases, select a clock phase among the plurality of locally-generated clock phases closest to an edge signal, and output a phase voting signal to indicate a transition clock phase closest to the detected edge signal; and

a data recovery unit operative to track whether a first symbol was received multiple times consecutively prior to the detected edge and to assign the detected edge to one of a current bit period and a subsequent bit period based upon said transition clock phase and a number of times saida ~~a~~ first symbol was consecutively received prior to a transition to a second symbol.

13. (Currently Amended) The edge processor according to claim 12, further including a phase picking logic circuit coupled to the synchronizer to determine saidan ~~an~~ average phase based on the phase voting signalsignals ~~signals~~ received from the synchronizer.

14. (Currently Amended) A computer system including a plurality of modular components communicating with each other, each of the modular components employing a receiving method to receive a modulated data signal from another modular component, said receiving method comprising:

tracking a transmitted clock with a plurality of locally-generated clock phases;

estimating an average phase of one or more ~~previously~~ detected edges in a data stream;

registering a pulse edge in the ~~received stream of~~ data stream, at a transition phase corresponding to one of said plurality of locally-generated clock phases, to detect the pulse edge;

determining whether a first symbol was received multiple times consecutively prior to the detected pulse edge; and

using the determination of whether said first symbol was received multiple times consecutively in a receiver decision process.

15. (Original) The computer system according to claim 14, wherein said determining includes determining whether the pulse edge registered during said registering step corresponds to a lone transition from a consecutive sequence of said first symbol to a second symbol.

16. (Original) The computer system according to claim 15, wherein said receiving method further comprises establishing a threshold number of consecutive symbols to precede any said lone transition.

17. (Currently Amended) The computer system according to claim 16, wherein, if the registered pulse edge is determined to correspond to said~~a~~ lone transition, said using comprises associating said registered pulse edge with a current bit period when a number of consecutively received symbols is below said threshold number of consecutive symbols and said transition phase precedes an eye opening formed in the ~~received~~ data stream~~signal~~.

18. (Currently Amended) The computer system according to claim 16, wherein, if the registered pulse edge is determined to correspond to saida lone transition, said using comprises associating said detected pulse edge with a subsequent bit period when a number of consecutively received symbols is below said threshold number of consecutive symbols and said transition phase is preceded by an eye opening formed in the ~~received~~ data streamsignal.

19. (Currently Amended) The computer system according to claim 16, wherein if the registered pulse edge is determined to correspond to saida lone transition, said using comprises associating said detected pulse edge with a current bit period when a number of consecutively received symbols exceeds said threshold number of consecutive symbols and an eye opening formed in the received data signal is between said transition phase and an immediately subsequent clock phase.

20. (Currently Amended) The computer system according to claim 14, wherein said determining includes determining whether the pulse edge registered during said registering step corresponds to a trailing edge of a single second symbol between a consecutive sequence of said first symbol and another occurrence of said first symbol.

21. (Currently Amended) The computer system according to claim 20, wherein said receiving method further comprises establishing a threshold number of consecutive symbols to precede saida single second symbol.

22. (Currently Amended) The computer system according to claim 21, wherein, if the registered pulse edge is determined to correspond to saida trailing edge of saida single second symbol, said using comprises associating said registered pulse edge with a current bit period when a number of consecutively received symbols is below said threshold number of consecutive symbols and said transition phase precedes an eye opening formed in the ~~received~~ data streamsignal.

23. (Currently Amended) The computer system method according to claim 21, wherein, if the registered pulse edge is determined to correspond to saida trailing edge of saida single second symbol, said using comprises associating said registered pulse edge with a subsequent bit period when a number of consecutively received symbols is below said threshold number of consecutive symbols and an eye opening formed in the ~~received~~ data streamsignal precedes the transition phase.

24. (Currently Amended) The computer system according to claim 21, wherein if the registered pulse edge is determined to correspond to saida trailing edge of saida single second symbol, said using comprises associating said registered pulse edge with a subsequent bit period when a number of consecutively received symbols exceeds said threshold number of consecutive symbols and an eye opening formed in the received data signal is between said transition phase and an immediately subsequent clock phase.

25. (Currently Amended) A computer readable media having instructions encoded thereon causing a processor to:

track a transmitted clock with a plurality of locally-generated clock phases;

estimate an average phase of one or more ~~previously~~ detected edges in a data stream;

register a pulse edge in the ~~received stream of~~ data stream, at a transition phase corresponding to one of said plurality of locally-generated clock phases, to detect the pulse edge;

determine whether a first symbol was received multiple times consecutively prior to the detected pulse edge; and

use the determination of whether said first symbol was received multiple times consecutively in a receiver decision process.

26. (Currently Amended) A computer system comprising:

a plurality of components communicating with each other, each of the components including a receiver to receive a modulated data signal from another component, said receiver further to:

track a transmitted clock with a plurality of locally-generated clock phases;

estimate an average phase of one or more ~~previously~~ detected edges in the modulated data signal;

register a pulse edge in the ~~received stream of~~ modulated data signal, at a transition phase corresponding to one of said plurality of locally-generated clock phases, to detect the pulse edge;

determine whether a first symbol was received multiple times consecutively prior to the detected pulse edge; and

use the determination of whether said first symbol was received multiple times consecutively in a receiver decision process.

27. (Withdrawn) In an edge-based receiver, a method for performing decisions comprising:

determining whether a last two bits are different and if a dead zone transition has occurred;

assigning a registered transition to a current bit period if the determination is true; and

assigning the registered transition to a next bit period if the determination is false.